Claims:

1. A communication diode driver circuit (CDDC) for selectively illuminating at least one communication diode (CD) in response to incoming digital data pulses, the communication diode driver circuit comprising:

at least one Communication Light Emitting Circuit (CLEC) having a Communication Light Emitting Branch (CLEB) with at least one CD, and designed to drive said CLEB at a nominal LED drive current I_N for selectively illuminating said at least one CD,

each CLEC of said at least one CLEC including a driver unit for combining a pulsed analog data voltage ADV(t) corresponding to the incoming digital data pulses, and a variable shift voltage SV(t) for issuing a pulsed drive voltage DV(t) for driving said CLEB with a pulsed LED drive current $I_{LED}(t)$ for selectively illuminating said at least one CD in accordance with the incoming digital data pulses, and

each CLEC of said at least one said CLEC including a closed loop feedback unit for tapping said CLEB for continuously monitoring a pulsed monitor voltage MV(t) directly proportional to said LED drive current $I_{LED}(t)$ for increasing said shift voltage SV(t) up to a maximum shift voltage SV_{max} less than a threshold drive voltage for continuously illuminating said at least one CD after a long absence of incoming digital data pulses, except for intermittently stepwise decreasing said shift voltage SV(t) in response to each single incoming digital data pulse contributing to a LED drive current satisfying the condition $I_{LED}(t)>I_N$.

2. The circuit according to Claim 1 wherein said feedback unit includes a toggle unit having a comparator for comparing a feedback voltage FV(t) derived from said monitor voltage MV(t) with a reference voltage V_{REF} proportional to the nominal LED drive current I_N for outputting a digital control state on the condition $I_{LED}(t)<I_N$, and an opposite OFF digital control state in response to each

single incoming digital data pulse contributing to a LED drive current satisfying the condition $I_{LED}(t)>I_N$.

3. The circuit according to Claim 2 wherein said toggle unit further includes a low pass filter (LPF) for shaping generally rectangular shaped pulses of said monitor voltage MV(t) to generally triangular shaped voltage pulses for determining the duration that said toggle unit issues said opposite digital control states on the condition $I_{LED}(t)>I_N$.

4. The circuit according to any one of Claims 1 to 3 wherein said feedback unit includes an integrating unit with a memory device for providing said shift voltage SV(t) wherein said memory device includes a memory component for continuously increasing said shift voltage SV(t) on the condition $I_{LED}(t)<I_N$.

5. The circuit according to Claim 4 wherein said memory component is a capacitive memory component.

6. The circuit according to Claim 5 wherein said memory device includes a resistive memory component for selectively discharging said capacitive memory component on the condition $I_{LED}(t)>I_N$.

7. The circuit according to any one of Claims 1 to 6 wherein said driver unit includes a shift amplifier for algebraically superimposing said analog data voltage ADV(t) and said shift voltage SV(t).

8. The circuit according to any one of Claims 1 to 7 wherein said CLEB includes a sense resistor tied to ground and said toggle unit taps said sense resistor for continuously monitoring said monitor voltage MV(t).